ABHINAV DATTA

+91 94924 86726 | abhi07janamaddi@gmail.com | | abhinav datta | LinkedIn
Github:- (Abhinav Datta) | Vijayawada, Andhra Pradesh, India

OBJECTIVE

Electronics Engineering undergraduate specialising in VLSI design, digital verification, and embedded IoT systems. Experienced in SystemVerilog testbench development, constrained-random functional verification, RTL simulation, and structured test planning. Actively building UVM methodology skills. Seeking a Silicon Design Verification or Embedded Systems internship to apply hardware verification fundamentals to real-world projects.

EXPERIENCE

Digital Design & Verification Intern | EdiGlobe | Vijayawada, India *[Jan 2025 - Mar 2025]*

- Accelerated simulation debug cycles by 30% by developing structured SystemVerilog testbenches to verify combinational and sequential logic across 3 digital circuit designs.
- Improved functional verification coverage to 90%+ by applying constrained-random stimulus techniques to validate logic gate behaviour against defined functional specifications.
- Reduced simulation error rate by 25% by systematically troubleshooting Verilog HDL models through waveform analysis, resolving timing and logic faults across all project milestones.
- Delivered all verification tasks 100% on schedule by following a structured test plan aligned with standard VLSI design verification flows.

IoT & Embedded Systems Intern | upSkill Campus / UniConverge Technologies | Vijayawada, India *[Feb 2026 - May 2026]*

- Designed and implemented a Smart Industrial Monitoring System using ESP8266 NodeMCU, DHT11, and MQ-2 sensors to track temperature, humidity, and gas levels in real time.
- Validated system performance through structured test cases, achieving stable Wi-Fi connectivity and under 2s alert response time across all monitored parameters.
- Integrated sensor data with Blynk Cloud platform, enabling remote dashboards and instant threshold alerts — demonstrating end-to-end hardware-to-cloud verification workflow.
- Strengthened project scalability by documenting a modular design flow supporting easy integration of additional sensors and IoT protocols (MQTT, HTTP).

Software Engineering Intern | Uptricks Services Pvt. Ltd. | Pune, India *[May 2026 - Present]*

- Improved module reliability by debugging logic errors across 3 active feature modules, reducing reported defects by 20% within the first month of joining.
- Strengthened code quality by implementing structured validation checks, ensuring 100% of assigned modules met functional specifications before release.

Additional: *Content Writer Intern, InAmigos Foundation (IAF) - Apr 2026 (2 weeks). Delivered 100% of assigned articles ahead of deadline.*

PROJECTS

VLSI Functional Verification - Combinational Circuit Simulation | SystemVerilog | Verilog HDL | Assertion-Based Verification

- Verified correctness of 4 combinational digital circuits by implementing RTL designs and simulating with self-checking testbenches, achieving 95% functional coverage.

- Reduced re-simulation iterations by 50% by catching design violations at simulation time using assertion-based checks, applying principles consistent with UVM methodology.

2-Digit Real-Time Decimal Counter | IC 7474 Flip-Flop | 555 Timer | Sequential Logic Design

- Designed and functionally verified a sequential counter using IC 7474 flip-flops and 555 timers, validated against a 10-state truth table with zero logic errors on first test run.

Priority-Based Digital Voting System | 7408 AND Gate | 7432 OR Gate | Breadboard Prototype

- Prototyped a priority-encoded voting circuit and verified correct output across all 8 input combinations during systematic functional testing.

Python Engineering Utilities | Python | Signal Processing | Engineering Computation

- Built 5 Python utilities automating engineering calculations including spectral analysis and logic validation, reducing manual computation time across coursework projects.

EDUCATION

B.Tech, Electronics and Communication Engineering | Velagapudi Ramakrishna Siddhartha Engineering College, Vijayawada | 2024 - Expected Jan 2028

Intermediate (Class XII) | SR Junior College, Vijayawada | Mar 2024 / *83.7%*

High School (Class X) | Narayana E.M High School, Vijayawada | May 2022 / *79.33%*

CERTIFICATIONS

EdiGlobe VLSI Design Certification | EdiGlobe | 2025

EdiGlobe Internship Completion Certificate | EdiGlobe | 2025

Spectral Analysis Techniques | NPTEL | 2025

Python Essentials 2 | Cisco Networking Academy | 2024

Problem Solving with C Programming Language | Online | 2024

SKILLS

Verification and HDL: SystemVerilog, Verilog HDL, Functional Verification, Testbench Development, Constrained-Random Verification, Assertion-Based Verification, VLSI Design, Digital Logic Design, RTL Simulation, UVM (in progress)

Embedded and IoT: ESP8266 NodeMCU, DHT11/MQ-2 Sensors, Blynk Cloud, MQTT, HTTP, Embedded C

Programming: Python, C, MATLAB, Java, JavaScript, HTML, CSS

Tools and Platforms: Linux (Ubuntu, Fedora), Android Studio, Git

Soft Skills: Technical Documentation, Structured Problem-Solving, Team Collaboration

LANGUAGES

English - Professional proficiency (STEP certified) | **Telugu** - Native | **Hindi** - Working proficiency